



Dual-Channel, Digital Isolators, Enhanced System-Level ESD Reliability

ADuM3200/ADuM3201

FEATURES

Enhanced system-level ESD performance per IEC 61000-4-x

Narrow body, 8-lead SOIC, Pb-free package

Low power operation

5 V operation

1.6 mA per channel maximum @ 0 Mbps to 2 Mbps

3.7 mA per channel maximum @ 10 Mbps

7.5 mA per channel maximum @ 25 Mbps

3 V operation

1.4 mA per channel maximum @ 0 Mbps to 2 Mbps

2.4 mA per channel maximum @ 10 Mbps

4.6 mA per channel maximum @ 25 Mbps

Bidirectional communication

3 V/5 V level translation

High temperature operation: 105°C

High data rate: dc to 25 Mbps (NRZ)

Precise timing characteristics

3 ns maximum pulse-width distortion

3 ns maximum channel-to-channel matching

High common-mode transient immunity: >25 kV/μs

Safety and regulatory approvals

UL recognition: 2500 V rms for 1 minute per UL 1577

CSA Component Acceptance Notice #5A

VDE Certificate of Conformity

DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01

DIN EN 60950 (VDE 0805): 2001-12; DIN EN 60950: 2000

$V_{IORM} = 560$ V peak

APPLICATIONS

Size-critical multichannel isolation

SPI® interface/data converter isolation

RS-232/RS-422/RS-485 transceiver isolation

Digital field bus isolation

GENERAL DESCRIPTION

The ADuM320x¹ are dual-channel, digital isolators based on Analog Devices' *iCoupler*® technology. Combining high speed CMOS and monolithic transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives such as optocoupler devices.

By avoiding the use of LEDs and photodiodes, *iCoupler* devices remove the design difficulties commonly associated with optocouplers. The typical optocoupler concerns regarding uncertain current transfer ratios, nonlinear transfer functions, and temperature and lifetime effects are eliminated with the simple *iCoupler* digital interfaces and stable performance characteristics. The need for external drivers and other discrete components is eliminated with these *iCoupler* products. Furthermore, *iCoupler* devices consume one-tenth to one-sixth the power of optocouplers at comparable signal data rates.

The ADuM320x isolators provide two independent isolation channels in a variety of channel configurations and data rates (see the Ordering Guide). Both parts operate with the supply voltage on either side ranging from 2.7 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling a voltage translation functionality across the isolation barrier. The ADuM320x isolators have a patented refresh feature that ensures dc correctness in the absence of input logic transitions and during power-up/power-down conditions.

In comparison to the ADuM120x isolators, the ADuM320x isolators contain various circuit and layout changes to provide increased capability relative to system-level IEC 61000-4-x testing (ESD, burst, surge). The precise capability in these tests for either the ADuM120x or ADuM320x products is strongly determined by the design and layout of the user's board or module. For more information, see [Application Note AN-793, ESD/Latch-Up Considerations with *iCoupler* Isolation Products](#).

¹ Protected by U.S. Patents 5,952,849; 6,873,065; and other pending patents.

FUNCTIONAL BLOCK DIAGRAMS

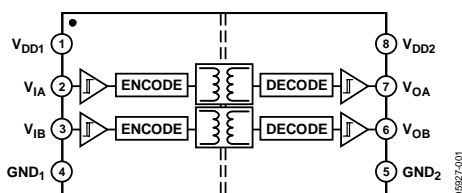


Figure 1. ADuM3200 Functional Block Diagram

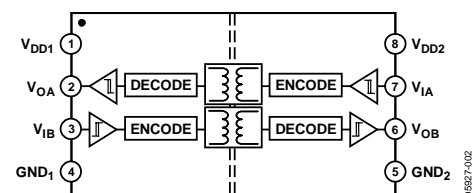


Figure 2. ADuM3201 Functional Block Diagram

Rev. 0

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ADuM3200/ADuM3201

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REVISION HISTORY

7/06—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All voltages are relative to their respective ground. $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$, $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = V_{DD2} = 5\text{ V}$.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current, per Channel, Quiescent	$I_{DD1(Q)}$		0.4	0.8	mA	
Output Supply Current, per Channel, Quiescent	$I_{DD0(Q)}$		0.5	0.6	mA	
ADuM3200, Total Supply Current, Two Channels ¹						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1(Q)}$		1.3	1.7	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(Q)}$		1.0	1.6	mA	DC to 1 MHz logic signal freq.
10 Mbps (BR and CR Grades Only)						
V_{DD1} Supply Current	$I_{DD1(10)}$		3.5	4.6	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(10)}$		1.7	2.8	mA	5 MHz logic signal freq.
25 Mbps (CR Grade Only)						
V_{DD1} Supply Current	$I_{DD1(25)}$		7.7	10.0	mA	12.5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(25)}$		3.1	3.9	mA	12.5 MHz logic signal freq.
ADuM3201, Total Supply Current, Two Channels ¹						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1(Q)}$		1.1	1.5	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(Q)}$		1.3	1.8	mA	DC to 1 MHz logic signal freq.
10 Mbps (BR and CR Grades Only)						
V_{DD1} Supply Current	$I_{DD1(10)}$		2.6	3.4	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(10)}$		3.1	4.0	mA	5 MHz logic signal freq.
25 Mbps (CR Grade Only)						
V_{DD1} Supply Current	$I_{DD1(25)}$		5.3	6.8	mA	12.5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(25)}$		6.4	8.3	mA	12.5 MHz logic signal freq.
For All Models						
Input Currents	I_{IA}, I_{IB}	-10	+0.01	+10	μA	$0 \leq V_{IA}, V_{IB} \leq V_{DD1}$ or V_{DD2}
Logic High Input Threshold	V_{IH}	0.7 V_{DD1} , V_{DD2}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DD1} , V_{DD2}	V	
Logic High Output Voltages	V_{OAH}	V_{DD1} , $V_{DD2} - 0.1$	5.0		V	$I_{Ox} = -20\ \mu\text{A}$, $V_{Ix} = V_{IxH}$
	V_{OBH}	V_{DD1} , $V_{DD2} - 0.5$	4.8		V	$I_{Ox} = -4\ \text{mA}$, $V_{Ix} = V_{IxH}$
Logic Low Output Voltages	V_{OAL}		0.0	0.1	V	$I_{Ox} = 20\ \mu\text{A}$, $V_{Ix} = V_{IxL}$
	V_{OBL}		0.04	0.1	V	$I_{Ox} = 400\ \mu\text{A}$, $V_{Ix} = V_{IxL}$
			0.2	0.4	V	$I_{Ox} = 4\ \text{mA}$, $V_{Ix} = V_{IxL}$
SWITCHING SPECIFICATIONS						
ADuM320xAR						
Minimum Pulse Width ²	PW			1000	ns	$C_L = 15\ \text{pF}$, CMOS signal levels
Maximum Data Rate ³		1			Mbps	$C_L = 15\ \text{pF}$, CMOS signal levels
Propagation Delay ⁴	t_{PHL}, t_{PLH}	20		150	ns	$C_L = 15\ \text{pF}$, CMOS signal levels
Pulse-Width Distortion, $ t_{PLH} - t_{PHL} $ ⁴	PWD			40	ns	$C_L = 15\ \text{pF}$, CMOS signal levels
Propagation Delay Skew ⁵	t_{PSK}			100	ns	$C_L = 15\ \text{pF}$, CMOS signal levels
Channel-to-Channel Matching ⁶	$t_{PSKCD/OD}$			50	ns	$C_L = 15\ \text{pF}$, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F		10		ns	$C_L = 15\ \text{pF}$, CMOS signal levels

ADuM3200/ADuM3201

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
ADuM320xBR						
Minimum Pulse Width ²	PW			100	ns	C _L = 15 pF, CMOS signal levels
Maximum Data Rate ³		10			Mbps	C _L = 15 pF, CMOS signal levels
Propagation Delay ⁴	t _{PHL} , t _{PLH}	20		50	ns	C _L = 15 pF, CMOS signal levels
Pulse-Width Distortion, t _{PLH} – t _{PHL} ⁴	PWD			3	ns	C _L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C _L = 15 pF, CMOS signal levels
Propagation Delay Skew ⁵	t _{PSK}			15	ns	C _L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels ⁶	t _{PSKCD}			3	ns	C _L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing Directional Channels ⁶	t _{PSKOD}			15	ns	C _L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t _R /t _F		2.5		ns	C _L = 15 pF, CMOS signal levels
ADuM320xCR						
Minimum Pulse Width ²	PW		20	40	ns	C _L = 15 pF, CMOS signal levels
Maximum Data Rate ³		25	50		Mbps	C _L = 15 pF, CMOS signal levels
Propagation Delay ⁴	t _{PHL} , t _{PLH}	20		45	ns	C _L = 15 pF, CMOS signal levels
Pulse-Width Distortion, t _{PLH} – t _{PHL} ⁴	PWD			3	ns	C _L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C _L = 15 pF, CMOS signal levels
Propagation Delay Skew ⁵	t _{PSK}			15	ns	C _L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels ⁶	t _{PSKCD}			3	ns	C _L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing Directional Channels ⁶	t _{PSKOD}			15	ns	C _L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t _R /t _F		2.5		ns	C _L = 15 pF, CMOS signal levels
For All Models						
Common-Mode Transient Immunity at Logic High Output ⁷	CM _H	25	35		kV/μs	V _{ix} = V _{DD1} , V _{DD2} , V _{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output ⁷	CM _L	25	35		kV/μs	V _{ix} = 0 V, V _{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f _r		1.2		Mbps	
Input Dynamic Supply Current, per Channel ⁸	I _{DDI} (D)		0.19		mA/Mbps	
Output Dynamic Supply Current, per Channel ⁸	I _{DDO} (D)		0.05		mA/Mbps	

¹ The supply current values for both channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 9 through Figure 11 for total I_{DD1} and I_{DD2} supply currents as a function of data rate for ADuM3200 and ADuM3201 channel configurations.

² The minimum pulse width is the shortest pulse width at which the specified pulse-width distortion is guaranteed.

³ The maximum data rate is the fastest data rate at which the specified pulse-width distortion is guaranteed.

⁴ t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{ix} signal to the 50% level of the falling edge of the V_{ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{ix} signal to the 50% level of the rising edge of the V_{ox} signal.

⁵ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

⁶ Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

⁷ CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD2}. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O < 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

⁸ Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in the signal data rate. See Figure 6 through Figure 8 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—3 V OPERATION

All voltages are relative to their respective ground. $2.7\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$, $2.7\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = V_{DD2} = 3.0\text{ V}$.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current, per Channel, Quiescent	$I_{DD1(Q)}$		0.3	0.5	mA	
Output Supply Current, per Channel, Quiescent	$I_{DDO(Q)}$		0.3	0.5	mA	
ADuM3200, Total Supply Current, Two Channels ¹						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1(Q)}$		0.8	1.3	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(Q)}$		0.7	1.0	mA	DC to 1 MHz logic signal freq.
10 Mbps (BR and CR Grades Only)						
V_{DD1} Supply Current	$I_{DD1(10)}$		2.0	3.2	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(10)}$		1.1	1.7	mA	5 MHz logic signal freq.
25 Mbps (CR Grade Only)						
V_{DD1} Supply Current	$I_{DD1(25)}$		4.3	6.4	mA	12.5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(25)}$		1.8	2.4	mA	12.5 MHz logic signal freq.
ADuM3201, Total Supply Current, Two Channels ¹						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1(Q)}$		0.7	1.3	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(Q)}$		0.8	1.6	mA	DC to 1 MHz logic signal freq.
10 Mbps (BR and CR Grades Only)						
V_{DD1} Supply Current	$I_{DD1(10)}$		1.5	2.1	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(10)}$		1.9	2.4	mA	5 MHz logic signal freq.
25 Mbps (CR Grade Only)						
V_{DD1} Supply Current	$I_{DD1(25)}$		3.0	4.2	mA	12.5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(25)}$		3.6	5.1	mA	12.5 MHz logic signal freq.
For All Models						
Input Currents	I_{IA}, I_{IB}	-10	+0.01	+10	μA	$0 \leq V_{IA}, V_{IB}, \leq V_{DD1}$ or V_{DD2}
Logic High Input Threshold	V_{IH}	$0.7V_{DD1},$ V_{DD2}			V	
Logic Low Input Threshold	V_{IL}			$0.3V_{DD1},$ V_{DD2}	V	
Logic High Output Voltages	V_{OAH}	$V_{DD1},$ $V_{DD2} - 0.1$	3.0		V	$I_{OX} = -20\ \mu\text{A}, V_{IX} = V_{IXH}$
	V_{OBH}	$V_{DD1},$ $V_{DD2} - 0.5$	2.8		V	$I_{OX} = -4\ \text{mA}, V_{IX} = V_{IXH}$
Logic Low Output Voltages	V_{OAL}		0.0	0.1	V	$I_{OX} = 20\ \mu\text{A}, V_{IX} = V_{IXL}$
	V_{OBL}		0.04	0.1	V	$I_{OX} = 400\ \mu\text{A}, V_{IX} = V_{IXL}$
			0.2	0.4	V	$I_{OX} = 4\ \text{mA}, V_{IX} = V_{IXL}$
SWITCHING SPECIFICATIONS						
ADuM320xAR						
Minimum Pulse Width ²	PW			1000	ns	$C_L = 15\ \text{pF}, \text{CMOS signal levels}$
Maximum Data Rate ³		1			Mbps	$C_L = 15\ \text{pF}, \text{CMOS signal levels}$
Propagation Delay ⁴	t_{PHL}, t_{PLH}	20		150	ns	$C_L = 15\ \text{pF}, \text{CMOS signal levels}$
Pulse-Width Distortion, $ t_{PLH} - t_{PHL} $ ⁴	PWD			40	ns	$C_L = 15\ \text{pF}, \text{CMOS signal levels}$
Propagation Delay Skew ⁵	t_{PSK}			100	ns	$C_L = 15\ \text{pF}, \text{CMOS signal levels}$
Channel-to-Channel Matching ⁶	$t_{PSKCD/OD}$			50	ns	$C_L = 15\ \text{pF}, \text{CMOS signal levels}$
Output Rise/Fall Time (10% to 90%)	t_R/t_F		10		ns	$C_L = 15\ \text{pF}, \text{CMOS signal levels}$

ADuM3200/ADuM3201

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
ADuM320xBR						
Minimum Pulse Width ²	PW			100	ns	C _L = 15 pF, CMOS signal levels
Maximum Data Rate ³		10			Mbps	C _L = 15 pF, CMOS signal levels
Propagation Delay ⁴	t _{PHL} , t _{PLH}	20		60	ns	C _L = 15 pF, CMOS signal levels
Pulse-Width Distortion, t _{PLH} – t _{PHL} ⁴	PWD			3	ns	C _L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C _L = 15 pF, CMOS signal levels
Propagation Delay Skew ⁵	t _{PSK}			22	ns	C _L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels ⁶	t _{PSKCD}			3	ns	C _L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing Directional Channels ⁶	t _{PSKOD}			22	ns	C _L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t _R /t _F		3.0		ns	C _L = 15 pF, CMOS signal levels
ADuM320xCR						
Minimum Pulse Width ²	PW		20	40	ns	C _L = 15 pF, CMOS signal levels
Maximum Data Rate ³		25	50		Mbps	C _L = 15 pF, CMOS signal levels
Propagation Delay ⁴	t _{PHL} , t _{PLH}	20		55	ns	C _L = 15 pF, CMOS signal levels
Pulse-Width Distortion, t _{PLH} – t _{PHL} ⁴	PWD			3	ns	C _L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C _L = 15 pF, CMOS signal levels
Propagation Delay Skew ⁵	t _{PSK}			16	ns	C _L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels ⁶	t _{PSKCD}			3	ns	C _L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing Directional Channels ⁶	t _{PSKOD}			16	ns	C _L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t _R /t _F		3.0		ns	C _L = 15 pF, CMOS signal levels
For All Models						
Common Mode Transient Immunity at Logic High Output ⁷	CM _H	25	35		kV/μs	V _{ix} = V _{DD1} , V _{DD2} , V _{CM} = 1000 V, transient magnitude = 800 V
Common Mode Transient Immunity at Logic Low Output ⁷	CM _L	25	35		kV/μs	V _{ix} = 0 V, V _{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f _r		1.1		Mbps	
Input Dynamic Supply Current, per Channel ⁸	I _{DDI (D)}		0.10		mA/Mbps	
Output Dynamic Supply Current, per Channel ⁸	I _{DDO (D)}		0.03		mA/Mbps	

¹ The supply current values for both channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 9 through Figure 11 for total I_{DD1} and I_{DD2} supply currents as a function of data rate for ADuM3200 and ADuM3201 channel configurations.

² The minimum pulse width is the shortest pulse width at which the specified pulse-width distortion is guaranteed.

³ The maximum data rate is the fastest data rate at which the specified pulse-width distortion is guaranteed.

⁴ t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{ix} signal to the 50% level of the falling edge of the V_{ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{ix} signal to the 50% level of the rising edge of the V_{ox} signal.

⁵ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

⁶ Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

⁷ CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD2}. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O < 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

⁸ Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in the signal data rate. See Figure 6 through Figure 8 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3 V OR 3 V/5 V OPERATION

All voltages are relative to their respective ground. 5 V/3 V operation: $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$. 3 V/5 V operation: $2.7\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$, $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at $T_A = 25^\circ\text{C}$; $V_{DD1} = 3.0\text{ V}$, $V_{DD2} = 5.0\text{ V}$; or $V_{DD1} = 5.0\text{ V}$, $V_{DD2} = 3.0\text{ V}$.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current, per Channel, Quiescent	$I_{DD1(Q)}$					
5 V/3 V Operation			0.4	0.8	mA	
3 V/5 V Operation			0.3	0.5	mA	
Output Supply Current, per Channel, Quiescent	$I_{DDO(Q)}$					
5 V/3 V Operation			0.3	0.5	mA	
3 V/5 V Operation			0.5	0.6	mA	
ADuM3200, Total Supply Current, Two Channels¹						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1(Q)}$					
5 V/3 V Operation			1.3	1.7	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			0.8	1.3	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(Q)}$					
5 V/3 V Operation			0.7	1.0	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.0	1.6	mA	DC to 1 MHz logic signal freq.
10 Mbps (BR and CR Grades Only)						
V_{DD1} Supply Current	$I_{DD1(10)}$					
5 V/3 V Operation			3.5	4.6	mA	5 MHz logic signal freq.
3 V/5 V Operation			2.0	3.2	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(10)}$					
5 V/3 V Operation			1.1	1.7	mA	5 MHz logic signal freq.
3 V/5 V Operation			1.7	2.8	mA	5 MHz logic signal freq.
25 Mbps (CR Grade Only)						
V_{DD1} Supply Current	$I_{DD1(25)}$					
5 V/3 V Operation			7.7	10.0	mA	12.5 MHz logic signal freq.
3 V/5 V Operation			4.3	6.4	mA	12.5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(25)}$					
5 V/3 V Operation			1.8	2.4	mA	12.5 MHz logic signal freq.
3 V/5 V Operation			3.1	3.9	mA	12.5 MHz logic signal freq.
ADuM3201, Total Supply Current, Two Channels¹						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1(Q)}$					
5 V/3 V Operation			1.1	1.5	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			0.7	1.3	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(Q)}$					
5 V/3 V Operation			0.8	1.6	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.3	1.8	mA	DC to 1 MHz logic signal freq.
10 Mbps (BR and CR Grades Only)						
V_{DD1} Supply Current	$I_{DD1(10)}$					
5 V/3 V Operation			2.6	3.4	mA	5 MHz logic signal freq.
3 V/5 V Operation			1.5	2.1	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(10)}$					
5 V/3 V Operation			1.9	2.4	mA	5 MHz logic signal freq.
3 V/5 V Operation			3.1	4.0	mA	5 MHz logic signal freq.

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Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
25 Mbps (CR Grade Only)						
V _{DD1} Supply Current	I _{DD1} (25)		5.3	6.8	mA	12.5 MHz logic signal freq.
5 V/3 V Operation			3.0	4.2	mA	12.5 MHz logic signal freq.
3 V/5 V Operation						
V _{DD2} Supply Current	I _{DD2} (25)		3.6	5.1	mA	12.5 MHz logic signal freq.
5 V/3 V Operation			6.4	8.3	mA	12.5 MHz logic signal freq.
3 V/5 V Operation						
For All Models						
Input Currents	I _{IA} , I _{IB}	-10	+0.01	+10	μA	0 ≤ V _{IA} , V _{IB} ≤ V _{DD1} or V _{DD2}
Logic High Input Threshold	V _{IH}	0.7 V _{DD1} , V _{DD2}			V	
Logic Low Input Threshold	V _{IL}			0.3 V _{DD1} , V _{DD2}	V	
5 V/3 V Operation		0.8			V	
3 V/5 V Operation		0.4			V	
Logic High Output Voltages	V _{OA} H, V _{OB} H	V _{DD1} , V _{DD2} - 0.1	V _{DD1} , V _{DD2}		V	I _{Ox} = -20 μA, V _{Ix} = V _{IxH}
		V _{DD1} , V _{DD2} - 0.5	V _{DD1} , V _{DD2} - 0.2		V	I _{Ox} = -4 mA, V _{Ix} = V _{IxH}
Logic Low Output Voltages	V _{OA} L, V _{OB} L		0.0	0.1	V	I _{Ox} = 20 μA, V _{Ix} = V _{IxL}
			0.04	0.1	V	I _{Ox} = 400 μA, V _{Ix} = V _{IxL}
			0.2	0.4	V	I _{Ox} = 4 mA, V _{Ix} = V _{IxL}
SWITCHING SPECIFICATIONS						
ADuM320xAR						
Minimum Pulse Width ²	PW			1000	ns	C _L = 15 pF, CMOS signal levels
Maximum Data Rate ³		1			Mbps	C _L = 15 pF, CMOS signal levels
Propagation Delay ⁴	t _{PHL} , t _{PLH}	15		150	ns	C _L = 15 pF, CMOS signal levels
Pulse-Width Distortion, t _{PLH} - t _{PHL} ⁴	PWD			40	ns	C _L = 15 pF, CMOS signal levels
Propagation Delay Skew ⁵	t _{PSK}			50	ns	C _L = 15 pF, CMOS signal levels
Channel-to-Channel Matching ⁶	t _{PSKCD} /OD			50	ns	C _L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t _R /t _F		10		ns	C _L = 15 pF, CMOS signal levels
ADuM320xBR						
Minimum Pulse Width ²	PW			100	ns	C _L = 15 pF, CMOS signal levels
Maximum Data Rate ³		10			Mbps	C _L = 15 pF, CMOS signal levels
Propagation Delay ⁴	t _{PHL} , t _{PLH}	15		55	ns	C _L = 15 pF, CMOS signal levels
Pulse-Width Distortion, t _{PLH} - t _{PHL} ⁴	PWD			3	ns	C _L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C _L = 15 pF, CMOS signal levels
Propagation Delay Skew ⁵	t _{PSK}			22	ns	C _L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels ⁶	t _{PSKCD}			3	ns	C _L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing Directional Channels ⁶	t _{PSKOD}			22	ns	C _L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t _R /t _F					
5 V/3 V Operation			3.0		ns	C _L = 15 pF, CMOS signal levels
3 V/5 V Operation			2.5		ns	C _L = 15 pF, CMOS signal levels

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
ADuM320xCR						
Minimum Pulse Width ²	PW		20	40	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Maximum Data Rate ³		25	50		Mbps	$C_L = 15 \text{ pF}$, CMOS signal levels
Propagation Delay ⁴	t_{PHL} , t_{PLH}	20		50	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Pulse-Width Distortion, $ t_{PLH} - t_{PHL} $ ⁴	PWD			3	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Change vs. Temperature			5		ps/°C	$C_L = 15 \text{ pF}$, CMOS signal levels
Propagation Delay Skew ⁵	t_{PSK}			15	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels ⁶	t_{PSKCD}			3	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Channel-to-Channel Matching, Opposing Directional Channels ⁶	t_{PSKOD}			15	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F					
5 V/3 V Operation			3.0		ns	$C_L = 15 \text{ pF}$, CMOS signal levels
3 V/5 V Operation			2.5		ns	$C_L = 15 \text{ pF}$, CMOS signal levels
For All Models						
Common-Mode Transient Immunity at Logic High Output ⁷	$ CM_H $	25	35		kV/ μ s	$V_{IX} = V_{DD1}, V_{DD2}, V_{CM} = 1000 \text{ V}$, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output ⁷	$ CM_L $	25	35		kV/ μ s	$V_{IX} = 0 \text{ V}, V_{CM} = 1000 \text{ V}$, transient magnitude = 800 V
Refresh Rate	f_r					
5 V/3 V Operation			1.2		Mbps	
3 V/5 V Operation			1.1		Mbps	
Input Dynamic Supply Current, per Channel ⁸	$I_{DD1(D)}$					
5 V/3 V Operation			0.19		mA/Mbps	
3 V/5 V Operation			0.10		mA/Mbps	
Output Dynamic Supply Current, per Channel ⁸	$I_{DDO(D)}$					
5 V/3 V Operation			0.03		mA/Mbps	
3 V/5 V Operation			0.05		mA/Mbps	

¹ The supply current values for both channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 9 through Figure 11 for total I_{DD1} and I_{DD2} supply currents as a function of data rate for ADuM3200 and ADuM3201 channel configurations.

² The minimum pulse width is the shortest pulse width at which the specified pulse-width distortion is guaranteed.

³ The maximum data rate is the fastest data rate at which the specified pulse-width distortion is guaranteed.

⁴ t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{IX} signal to the 50% level of the falling edge of the V_{OX} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{IX} signal to the 50% level of the rising edge of the V_{OX} signal.

⁵ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

⁶ Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

⁷ CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8 V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8 \text{ V}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

⁸ Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in the signal data rate. See Figure 6 through Figure 8 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating per-channel supply current for a given data rate.

ADuM3200/ADuM3201

PACKAGE CHARACTERISTICS

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input to Output) ¹	R _{I-O}		10 ¹²		Ω	f = 1 MHz
Capacitance (Input to Output) ¹	C _{I-O}		1.0		pF	
Input Capacitance	C _I		4.0		pF	
IC Junction-to-Case Thermal Resistance, Side 1	θ _{JCI}		46		°C/W	Thermocouple located at center of package underside
IC Junction-to-Case Thermal Resistance, Side 2	θ _{JCO}		41		°C/W	

¹ The device is considered a 2-terminal device; Pin 1, Pin 2, Pin 3, and Pin 4 are shorted together, and Pin 5, Pin 6, Pin 7, and Pin 8 are shorted together.

REGULATORY INFORMATION

The ADuM3200/ADuM3201 is approved by the following organizations.

Table 5.

UL	CSA	VDE
Recognized under 1577 Component Recognition Program ¹ 2500 V rms isolation voltage File E214100	Approved under CSA Component Acceptance Notice #5A File 205078	Certified according to DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01 ² Basic insulation, 560 V peak File 2471900-4880-0001

¹ In accordance with UL1577, each ADuM320x is proof-tested by applying an insulation test voltage ≥ 3000 V rms for 1 second (current leakage detection limit = 5 μA).

² In accordance with DIN EN 60747-5-2, each ADuM320x is proof-tested by applying an insulation test voltage ≥ 1050 V peak for 1 second (partial discharge detection limit = 5 pC).

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 6.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	4.90 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	4.01 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN EN 60747-5-2 (VDE 0884 PART 2) INSULATION CHARACTERISTICS

Table 7.

Description	Symbol	Characteristic	Unit
Installation Classification Per DIN VDE 0110 For Rated Mains Voltage ≤ 150 V rms For Rated Mains Voltage ≤ 300 V rms For Rated Mains Voltage ≤ 400 V rms		I–IV I–III I–II	
Climatic Classification		40/105/21	
Pollution Degree (DIN VDE 0110, Table 1)		2	
Maximum Working Insulation Voltage	V _{IORM}	560	V peak
Input-to-Output Test Voltage, Method b1 V _{IORM} × 1.875 = V _{PR} , 100% Production Test, t _m = 1 sec, Partial Discharge < 5 pC	V _{PR}	1050	V peak
Input-to-Output Test Voltage, Method a After Environmental Tests Subgroup 1 V _{IORM} × 1.6 = V _{PR} , t _m = 60 sec, Partial Discharge < 5 pC After Input and/or Safety Test Subgroup 2/3 V _{IORM} × 1.2 = V _{PR} , t _m = 60 sec, Partial Discharge < 5 pC	V _{PR}	896 672	V peak V peak
Highest Allowable Overvoltage (Transient Overvoltage, t _{TR} = 10 sec)	V _{TR}	4000	V peak
Safety-Limiting Values (Maximum Value Allowed in the Event of a Failure; also See Figure 3)			
Case Temperature	T _S	150	°C
Side 1 Current	I _{S1}	160	mA
Side 2 Current	I _{S2}	170	mA
Insulation Resistance at T _S , V _{IO} = 500 V	R _S	>10 ⁹	Ω

Note that the “*” marking on the package denotes DIN EN 60747-5-2 approval for a 560 V peak working voltage.

This isolator is suitable for basic isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits.

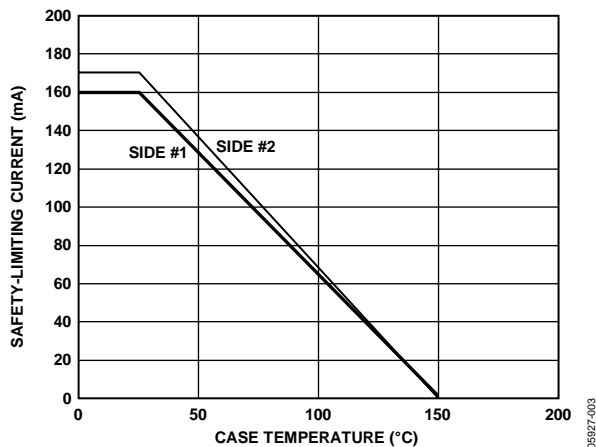


Figure 3. Thermal Derating Curve, Dependence of Safety-Limiting Values on Case Temperature, per DIN EN 60747-5-2

RECOMMENDED OPERATING CONDITIONS

Table 8.

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-40	+105	°C
Supply Voltages ¹	V _{DD1} , V _{DD2}	2.7	5.5	V
Input Signal Rise and Fall Times			1.0	ms

¹ All voltages are relative to their respective ground. See the DC Correctness and Magnetic Field Immunity section for information on immunity to external magnetic fields.

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ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 9.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{ST}	-55	+150	°C
Ambient Operating Temperature	T_A	-40	+105	°C
Supply Voltages ¹	V_{DD1}, V_{DD2}	-0.5	+7.0	V
Input Voltage ^{1, 2}	V_{IA}, V_{IB}	-0.5	$V_{DD1} + 0.5$	V
Output Voltage ^{1, 2}	V_{OA}, V_{OB}	-0.5	$V_{DDO} + 0.5$	V
Average Output Current, per Pin ³	I_O	-35	+35	mA
Common-Mode Transients ⁴	CM_H, CM_L	-100	+100	kV/μs

¹ All voltages are relative to their respective ground.

² V_{DD1} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively.

³ See Figure 3 for maximum rated current values for various temperatures.

⁴ Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the Absolute Maximum Rating can cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; Functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



Table 10. ADuM3200 Truth Table (Positive Logic)

V_{IA} Input	V_{IB} Input	V_{DD1} State	V_{DD2} State	V_{OA} Output	V_{OB} Output	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	X	Unpowered	Powered	H	H	Outputs return to the input state within 1 μs of V_{DD1} power restoration.
X	X	Powered	Unpowered	Indeterminate	Indeterminate	Outputs return to the input state within 1 μs of V_{DDO} power restoration.

Table 11. ADuM3201 Truth Table (Positive Logic)

V_{IA} Input	V_{IB} Input	V_{DD1} State	V_{DD2} State	V_{OA} Output	V_{OB} Output	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	X	Unpowered	Powered	Indeterminate	H	Outputs return to the input state within 1 μs of V_{DD1} power restoration.
X	X	Powered	Unpowered	H	Indeterminate	Outputs return to the input state within 1 μs of V_{DDO} power restoration.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

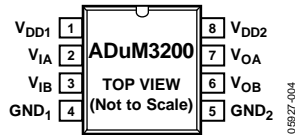


Figure 4. ADuM3200 Pin Configuration

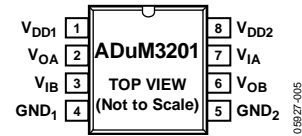


Figure 5. ADuM3201 Pin Configuration

Table 12. ADuM3200 Pin Function Descriptions

Pin No.	Mnemonic	Function
1	V _{DD1}	Supply Voltage for Isolator Side 1, 2.7V to 5.5 V.
2	V _{IA}	Logic Input A.
3	V _{IB}	Logic Input B.
4	GND ₁	Ground 1. Ground reference for Isolator Side 1.
5	GND ₂	Ground 2. Ground reference for Isolator Side 2.
6	V _{OB}	Logic Output B.
7	V _{OA}	Logic Output A.
8	V _{DD2}	Supply Voltage for Isolator Side 2, 2.7V to 5.5 V.

Table 13. ADuM3201 Pin Function Descriptions

Pin No.	Mnemonic	Function
1	V _{DD1}	Supply Voltage for Isolator Side 1, 2.7V to 5.5 V.
2	V _{OA}	Logic Output A.
3	V _{IB}	Logic Input B.
4	GND ₁	Ground 1. Ground reference for Isolator Side 1.
5	GND ₂	Ground 2. Ground reference for Isolator Side 2.
6	V _{OB}	Logic Output B.
7	V _{IA}	Logic Input A.
8	V _{DD2}	Supply Voltage for Isolator Side 2, 2.7V to 5.5 V.

TYPICAL PERFORMANCE CHARACTERISTICS

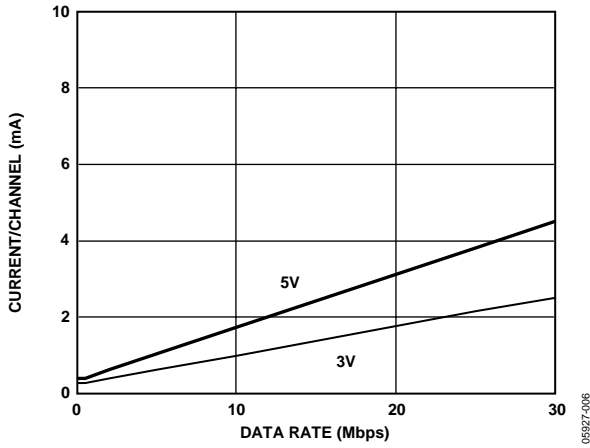


Figure 6. Typical Input Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation

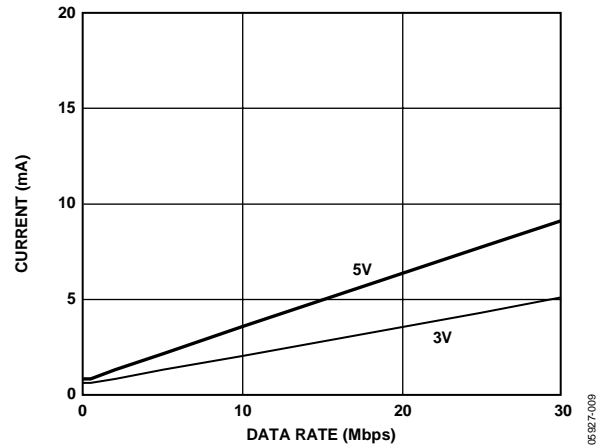


Figure 9. Typical ADuM3200 V_{DD1} Supply Current vs. Data Rate for 5 V and 3 V Operation

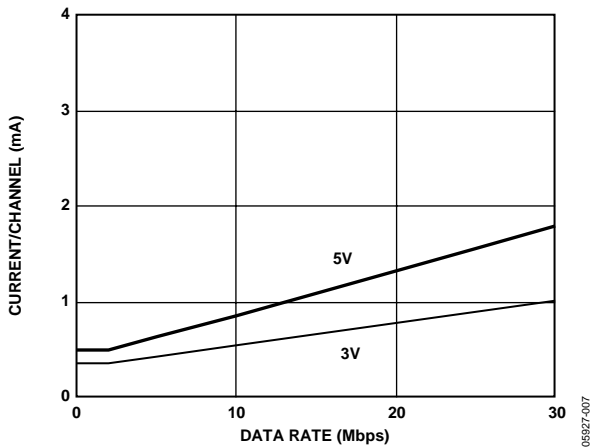


Figure 7. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (No Output Load)

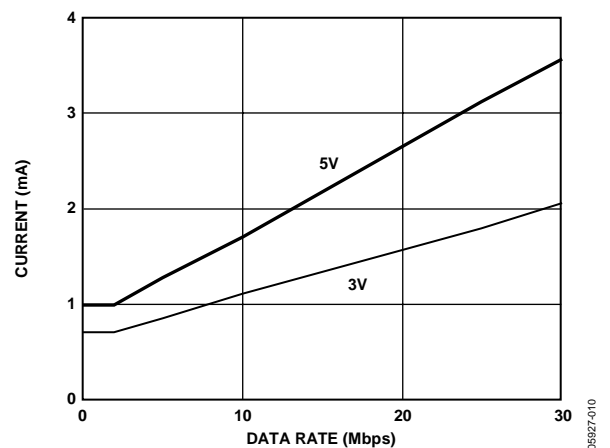


Figure 10. Typical ADuM3200 V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

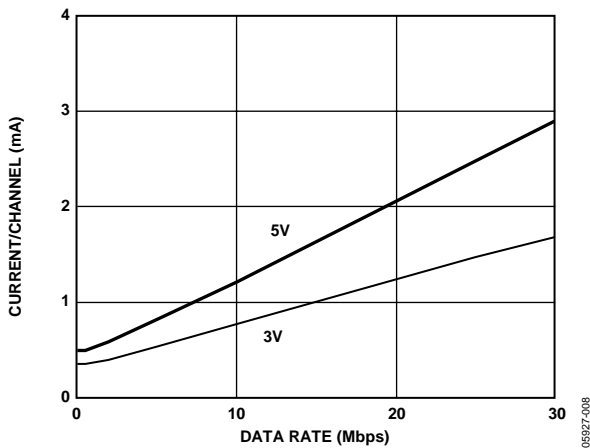


Figure 8. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (15 pF Output Load)

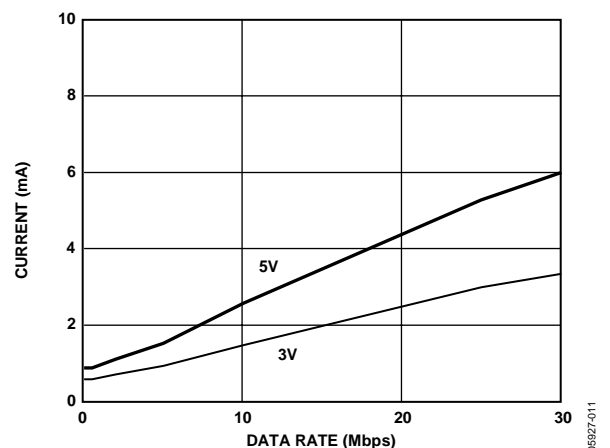


Figure 11. Typical ADuM3201 V_{DD1} or V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

APPLICATION INFORMATION

PC BOARD LAYOUT

The ADuM320x digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins. The capacitor value should be between 0.01 μF and 0.1 μF . The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm.

SYSTEM-LEVEL ESD CONSIDERATIONS AND ENHANCEMENTS

System-level ESD reliability (for example, per IEC 61000-4-x) is highly dependent on system design which varies widely by application. The ADuM320x incorporate many enhancements to make ESD reliability less dependent on system design. The enhancements include:

- ESD protection cells added to all input/output interfaces.
- Key metal trace resistances reduced using wider geometry and paralleling of lines with vias.
- The SCR effect inherent in CMOS devices minimized by use of guarding and isolation technique between PMOS and NMOS devices.
- Areas of high electric field concentration eliminated using 45° corners on metal traces.
- Supply pin overvoltage prevented with larger ESD clamps between each supply pin and its respective ground.

While the ADuM320x improve system-level ESD reliability, they are no substitute for a robust system-level design. See [Application Note AN-793, ESD/Latch-Up Considerations with iCoupler Isolation Products](#) for detailed recommendations on board layout and system-level design.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic low output can differ from the propagation delay to a logic high.

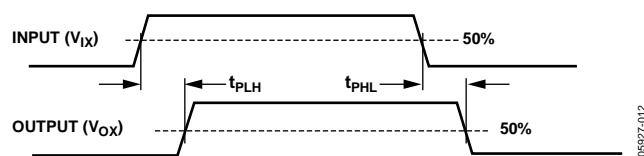


Figure 12. Propagation Delay Parameters

Pulse-width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the input signal's timing is preserved.

Channel-to-channel matching refers to the maximum amount that the propagation delay differs between channels within a single ADuM320x component.

Propagation delay skew refers to the maximum amount that the propagation delay differs between multiple ADuM320x components operating under the same conditions.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is therefore either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions of more than 2 μs at the input, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than about 5 μs , the input side is assumed to be unpowered or nonfunctional, in which case, the isolator output is forced to a default state (see Table 8) by the watchdog timer circuit.

The ADuM320x are extremely immune to external magnetic fields. The limitation on the ADuM320x's magnetic field immunity is set by the condition in which induced voltage in the transformer's receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3 V operating condition of the ADuM320x is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, therefore establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt) \sum \pi r_n^2, n = 1, 2, \dots, N$$

where:

β is the magnetic flux density (gauss).

N is the number of turns in the receiving coil.

r_n is the radius of the n th turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADuM320x and an imposed requirement that the induced voltage be at most 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 13.

ADuM3200/ADuM3201

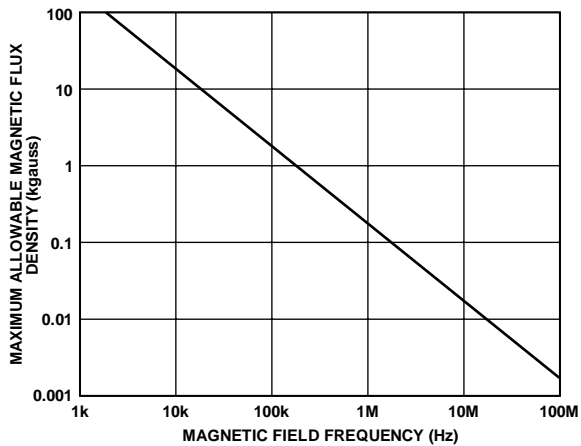


Figure 13. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event were to occur during a transmitted pulse (and had the worst-case polarity), it would reduce the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM320x transformers. Figure 14 expresses these allowable current magnitudes as a function of frequency for selected distances. As seen, the ADuM320x are extremely immune and can be affected only by extremely large currents operated at high frequency and very close to the component. For the 1 MHz example, one would have to place a 0.5 kA current 5 mm away from the ADuM320x to affect the component's operation.

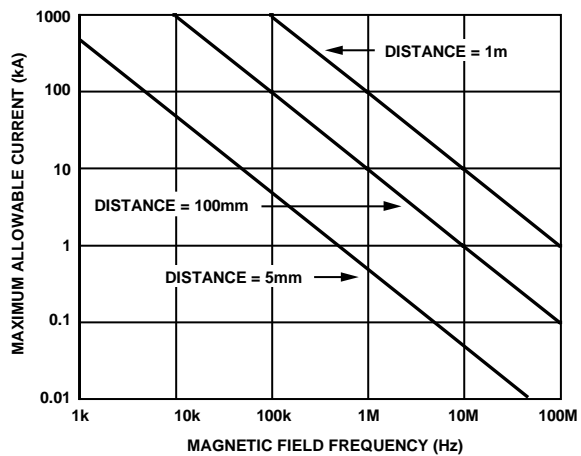


Figure 14. Maximum Allowable Current for Various Current-to-ADuM320x Spacings

Note that at combinations of strong magnetic fields and high frequencies, any loops formed by printed circuit board traces could induce sufficiently large error voltages to trigger the threshold of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

POWER CONSUMPTION

The supply current at a given channel of the ADuM320x isolator is a function of the supply voltage, the channel's data rate, and the channel's output load.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI(Q)} \quad f \leq 0.5f_r$$

$$I_{DDI} = I_{DDI(D)} \times (2f - f_r) + I_{DDI(Q)} \quad f > 0.5f_r$$

for each output channel, the supply current is given by

$$I_{DDO} = I_{DDO(Q)} \quad f \leq 0.5f_r$$

$$I_{DDO} = (I_{DDO(D)} + (0.5 \times 10^{-3}) \times C_L V_{DDO}) \times (2f - f_r) + I_{DDO(Q)} \quad f > 0.5f_r$$

where:

$I_{DDI(D)}$, $I_{DDO(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).

C_L is the output load capacitance (pF).

V_{DDO} is the output supply voltage (V).

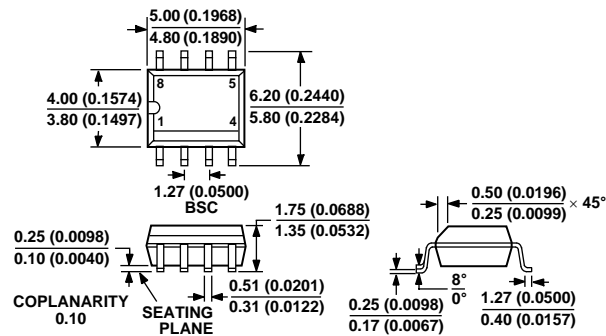
f is the input logic signal frequency (MHz, half of the input data rate, NRZ signaling).

f_r is the input stage refresh rate (Mbps).

$I_{DDI(Q)}$, $I_{DDO(Q)}$ are the specified input and output quiescent supply currents (mA).

To calculate the total I_{DD1} and I_{DD2} supply current, the supply currents for each input and output channel corresponding to I_{DD1} and I_{DD2} are calculated and totaled. Figure 6 provides per-channel input supply currents as a function of data rate. Figure 7 and Figure 8 provide per-channel output supply currents as a function of data rate for an unloaded output condition and for a 15 pF output condition, respectively. Figure 9 through Figure 11 provide total I_{DD1} and I_{DD2} supply current as a function of data rate for ADuM3200 and ADuM3201 channel configurations.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 15. 8-Lead Standard Small Outline Package [SOIC_N] Narrow Body (R-8)

Dimensions shown in millimeters (inches)

ORDERING GUIDE

Model	Number of Inputs, V _{DD1} Side	Number of Inputs, V _{DD2} Side	Maximum Data Rate (Mbps)	Maximum Propagation Delay, 5 V (ns)	Maximum Pulse-Width Distortion (ns)	Temperature Range (°C)	Package Option ¹
ADuM3200ARZ ²	2	0	1	150	40	-40 to +105	R-8
ADuM3200ARZ-RL7 ²	2	0	1	150	40	-40 to +105	R-8
ADuM3200BRZ ²	2	0	10	50	3	-40 to +105	R-8
ADuM3200BRZ-RL7 ²	2	0	10	50	3	-40 to +105	R-8
ADuM3200CRZ ²	2	0	25	45	3	-40 to +105	R-8
ADuM3200CRZ-RL7 ²	2	0	25	45	3	-40 to +105	R-8
ADuM3201ARZ ²	1	1	1	150	40	-40 to +105	R-8
ADuM3201ARZ-RL7 ²	1	1	1	150	40	-40 to +105	R-8
ADuM3201BRZ ²	1	1	10	50	3	-40 to +105	R-8
ADuM3201BRZ-RL7 ²	1	1	10	50	3	-40 to +105	R-8
ADuM3201CRZ ²	1	1	25	45	3	-40 to +105	R-8
ADuM3201CRZ-RL7 ²	1	1	25	45	3	-40 to +105	R-8

¹ R-8 = 8-lead narrow body SOIC_N.

² Z = Pb-free part.

ADuM3200/ADuM3201

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ADuM3200/ADuM3201

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